



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Re application of: Isahi Nachumovsky

Application No.: 09/975,049

Group No.: 2814

Filed: 10/10/2001

Examiner: Howard Weiss

For: "TWO-BIT SPLIT-GATE NON-VOLATILE MEMORY TRANSISTOR"

**Docket No.: TSI 105**

Assistant Commissioner for Patents  
Washington, D.C. 20231-0001

Date: October 14, 2002


**AMENDMENT TRANSMITTAL**

- Transmitted herewith is an amendment for this application.
- STATUS:** Applicant is other than a small entity.
- EXTENSION OF TERM:** A Petition And Fee For Extension Of Time (37.C.F.R. 1.136(a)) is filed herewith.
- FEE FOR CLAIMS:** The fee for claims (37 C.F.R. 1.16(b)-(d)) has been calculated below:

	(Col.1)		(Col. 2)	(Col. 3)	LARGE ENTITY	
	Claims Remaining After Amendment		Highest No. Previously Paid For	Present Extra	Rate	Addit. Fee
Total	19	Minus	20	= 0	x \$18 =	\$0.00
Indep.	2	Minus	3	= 0	x \$84 =	\$0.00
First Presentation of Multiple Dependent Claim					+ \$280 =	\$0
Total					Addit. Fee	\$0.00

- FEE PAYMENT and DEFICIENCY:** Please charge Deposit Acct. 50-0574 the amount of \$110.00 for 1-month extension of time. If any additional extension and/or fee is required, also charge Account No. 50-0574.

Customer No. 022888  
Tel.: (925) 895-3545

  
**SIGNATURE OF PRACTITIONER**  
E. Eric Hoffman  
Reg. No. 38,186

I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C., 20231, on 10/14/2002.

Date: Oct. 14, 2002

Signature: Carrie Redolick



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TECHNOLOGY CENTER 2800IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor: Ishai Nachumovsky  
Assignee: Tower Semiconductor, Ltd.  
Title: TWO-BIT SPLIT-GATE NON-VOLATILE MEMORY TRANSISTOR  
Serial No.: 09/975,049      Group No.: 2814  
Filed: 10/10/2001      Examiner: Howard Weiss  
Docket No.: TSL-105

October 14, 2002  
San Jose, California

Assistant Commissioner for Patents  
Washington, D.C. 20231-0001

RESPONSE TO FIRST OFFICE ACTION

Sir:

Applicant submits the following remarks in response to the Office Action dated June 14, 2002. A petition for a 1-month extension, extending the period for response to October 14, 2002, accompanies the present response.

IN THE SPECIFICATION

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[0028] As illustrated in Fig. 4, array 100 is fabricated in a semiconductor region 401. In the described embodiment, semiconductor region 401 is a p-type well formed in a monocrystalline silicon substrate. Semiconductor region 401 has a dopant concentration of about  $5 \times 10^{16}$ - $2 \times 10^{17}$  atoms/cm<sup>2</sup>. In other embodiments, semiconductor region 401 can be a p-type silicon substrate. Field oxide 402 is thermally grown at the upper surface of substrate 401 using a conventional local oxidation of silicon (LOCOS) process. In the described embodiment, field oxide 402 is grown to a thickness in the range of about 4000 to 8000 Å. In the described embodiment, the field oxide is grown to a